US 20080150434A1

(19) **United States**

(12) **Patent Application Publication**

(10) **Pub. No.: US 2008/0150434 A1**

(43) **Pub. Date: Jun. 26, 2008**

SUNG et al.

(54) **DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

(75) Inventors: **Un-cheol SUNG**, Anyang-si (KR); **Jin-koo CHUNG**, Suwon-si (KR); **Jung-soo RHEE**, Seoul (KR)

Correspondence Address:
CANTOR COLBURN, LLP
20 Church Street, 22nd Floor
Hartford, CT 06103

(73) Assignee: **SAMSUNG ELECTRONICS CO., LTD.**, Suwon-si (KR)

(21) Appl. No.: **11/843,210**

(22) Filed: **Aug. 22, 2007**

(30) **Foreign Application Priority Data**

Dec. 26, 2006 (KR) 10-2006-0134186

Publication Classification

(51) **Int. Cl.**
G09G 3/10 (2006.01)
H01L 21/84 (2006.01)

(52) **U.S. Cl.** **315/169.3**; 438/23; 257/E21.7

(57) **ABSTRACT**

A display device includes; an insulating substrate, a thin film transistor disposed on the insulating substrate and which comprises a drain electrode, a wall disposed on the thin film transistor and which includes an opening and a contact hole which exposes the drain electrode, a pixel electrode connected to the drain electrode through the contact hole and which comprises a first part in direct contact with the insulating substrate and a second part connected to the first part, an organic layer disposed on the pixel electrode and which comprises an organic emission layer, and a common electrode disposed on the organic layer

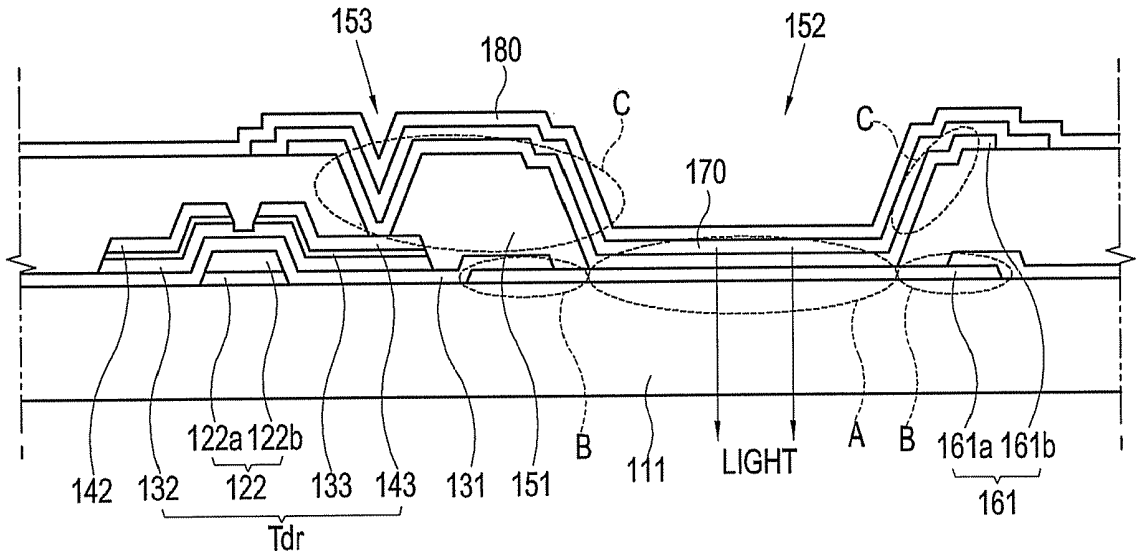


FIG. 1

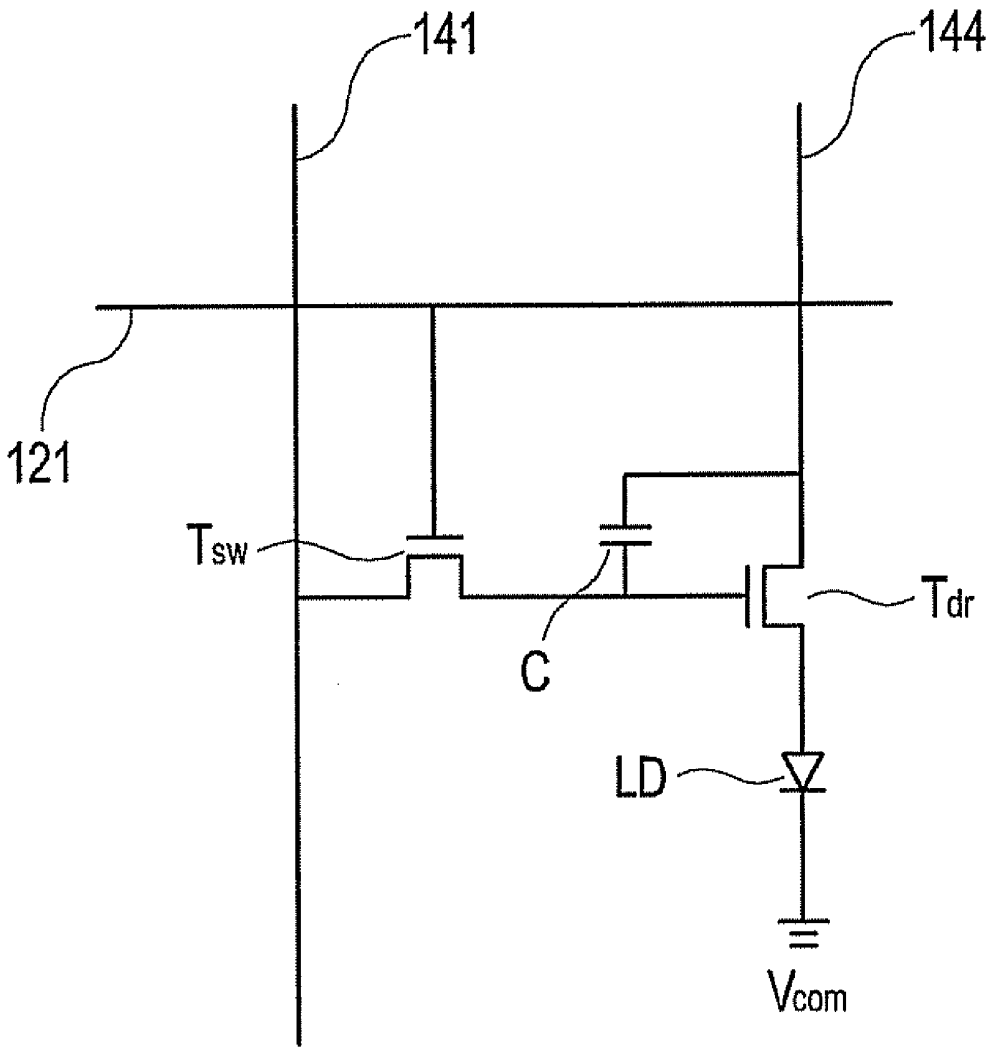


FIG. 2

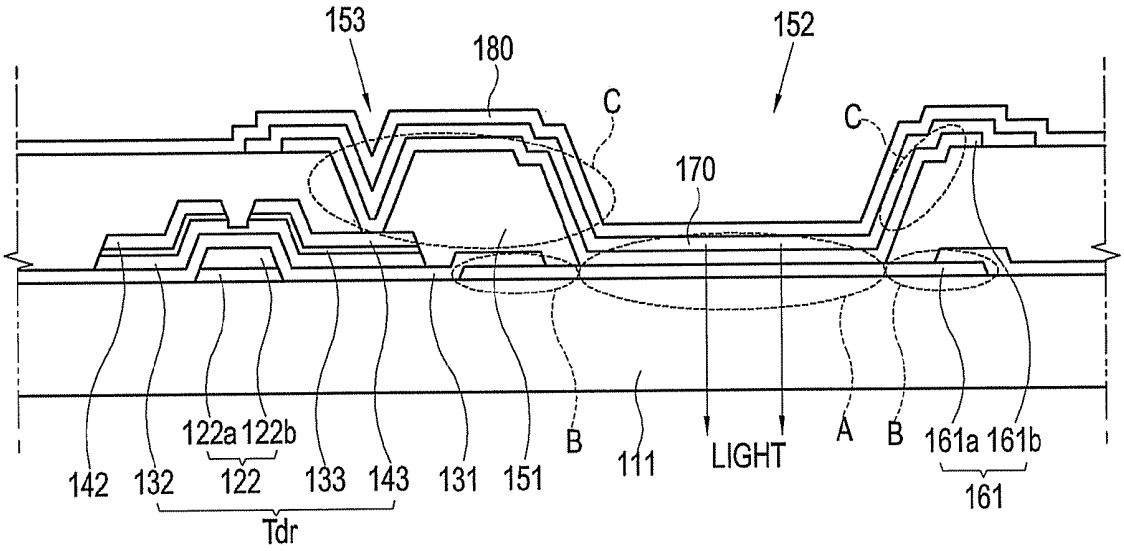

153
180
152
C
C
170
122a 122b
142
132
122
133
143
131
151
B
111
LIGHT
A
B
161a 161b
161
Tdr

FIG. 3A

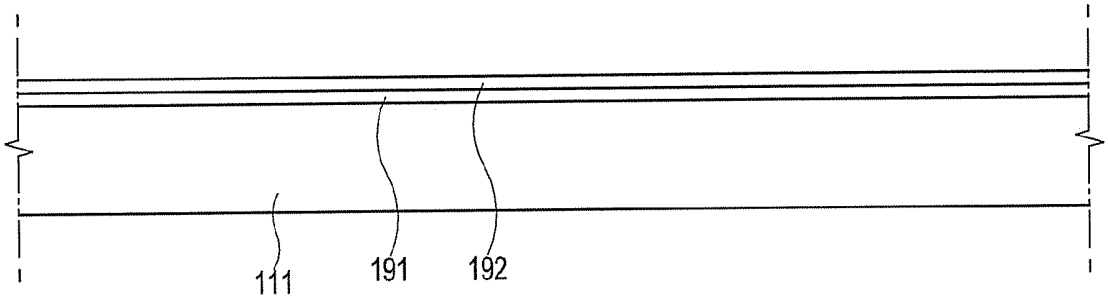


FIG. 3B

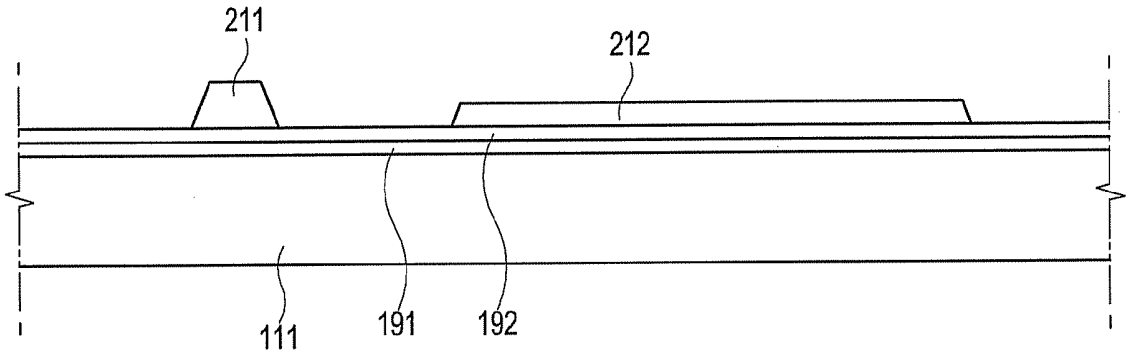


FIG. 3C

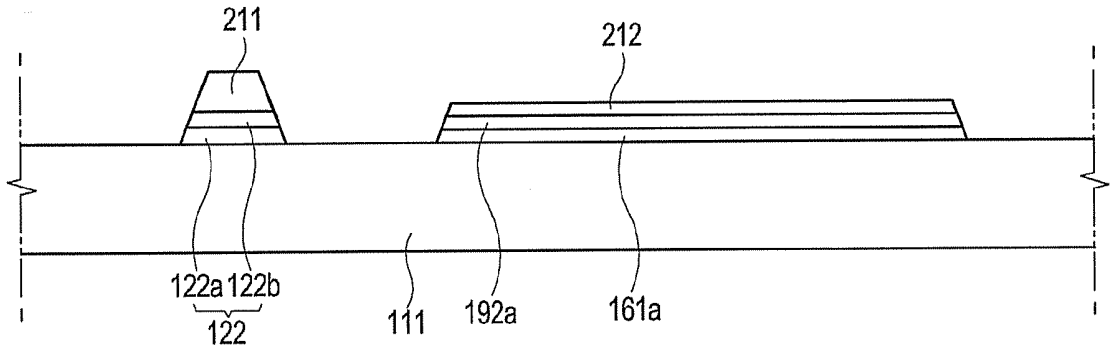


FIG. 3D

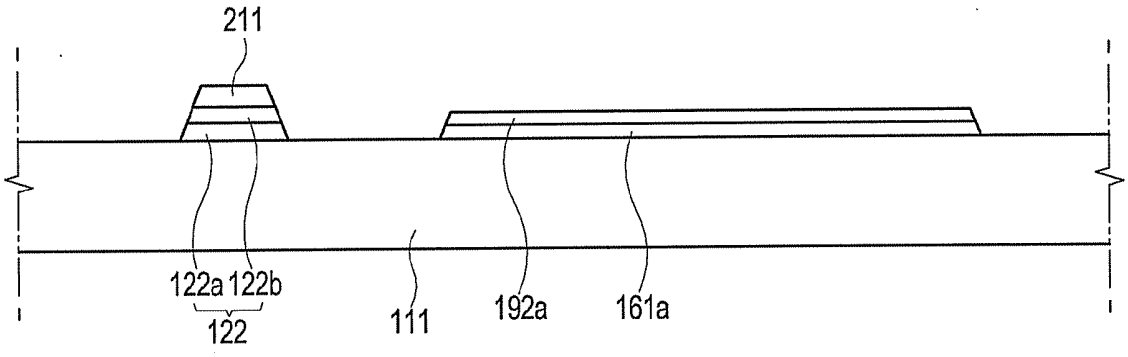


FIG. 3E

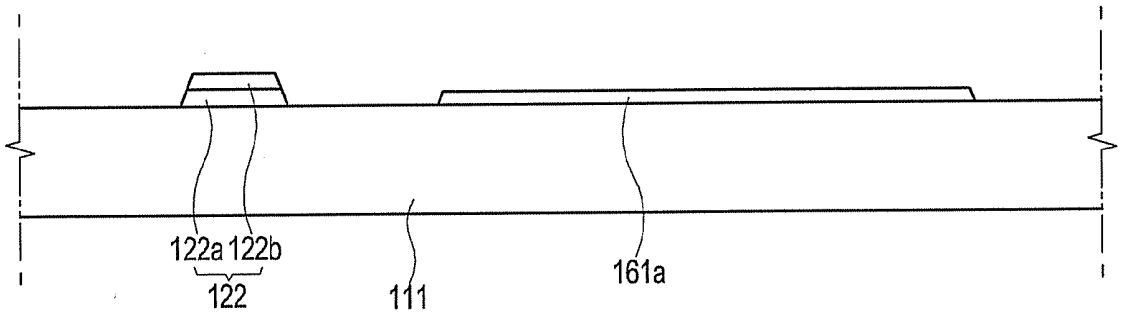


FIG. 3F

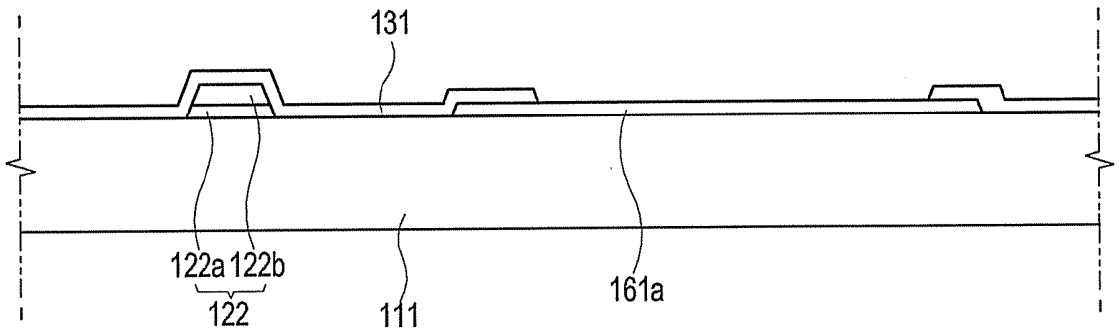


FIG. 3G

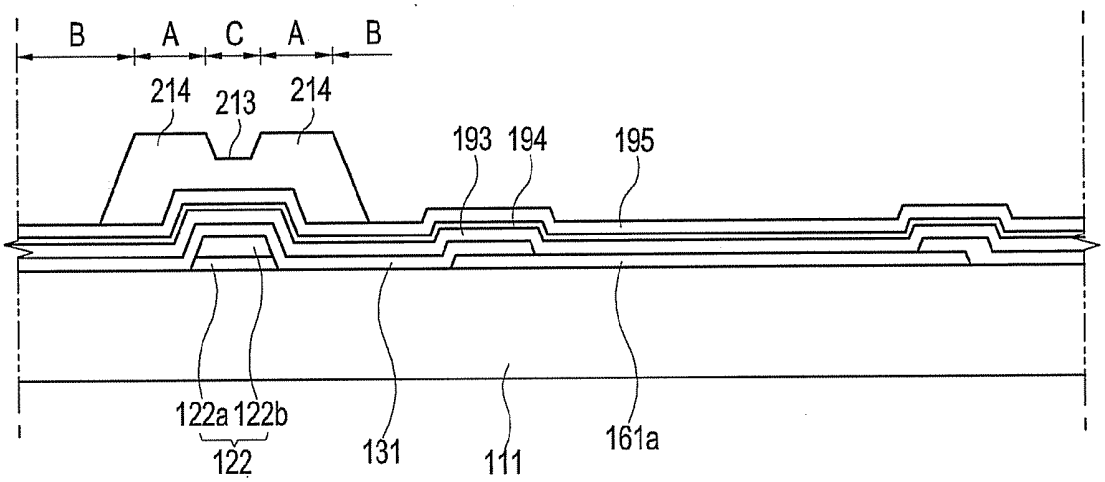


FIG. 3H

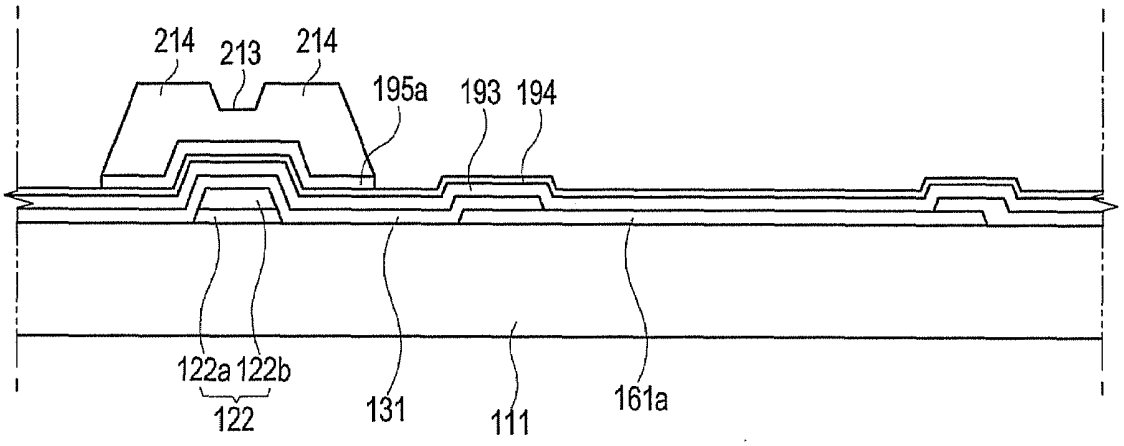


FIG. 3I

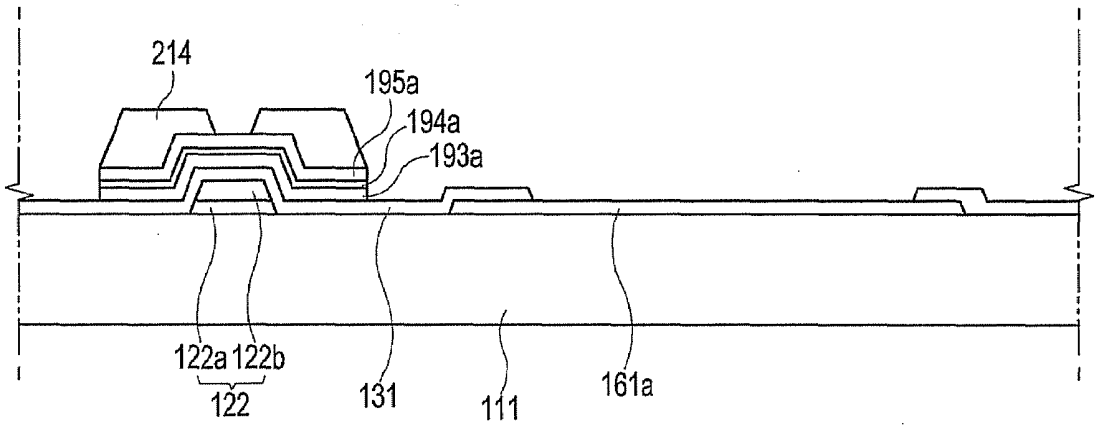


FIG. 3J

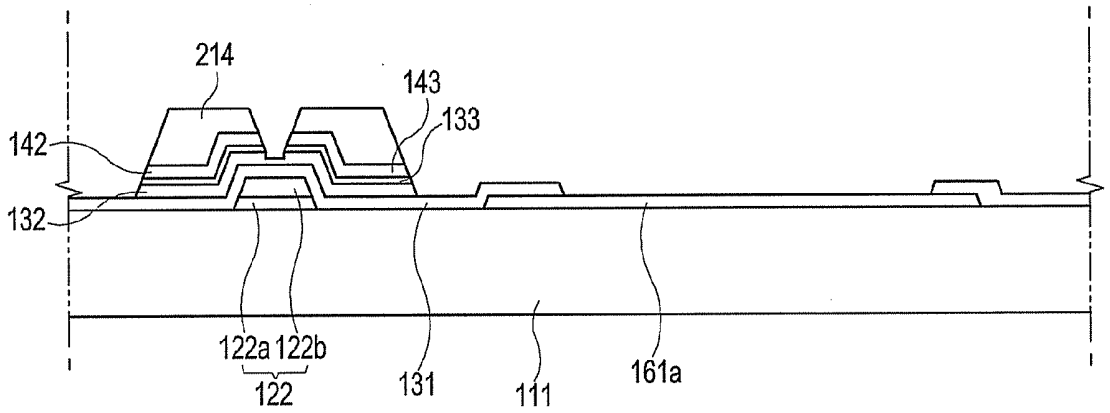


FIG. 3K

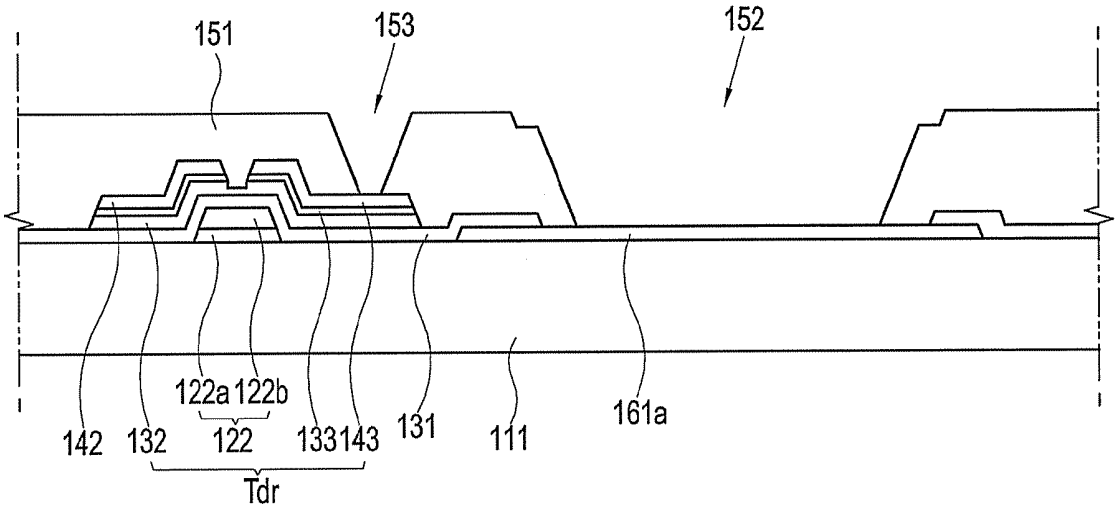


FIG. 3L

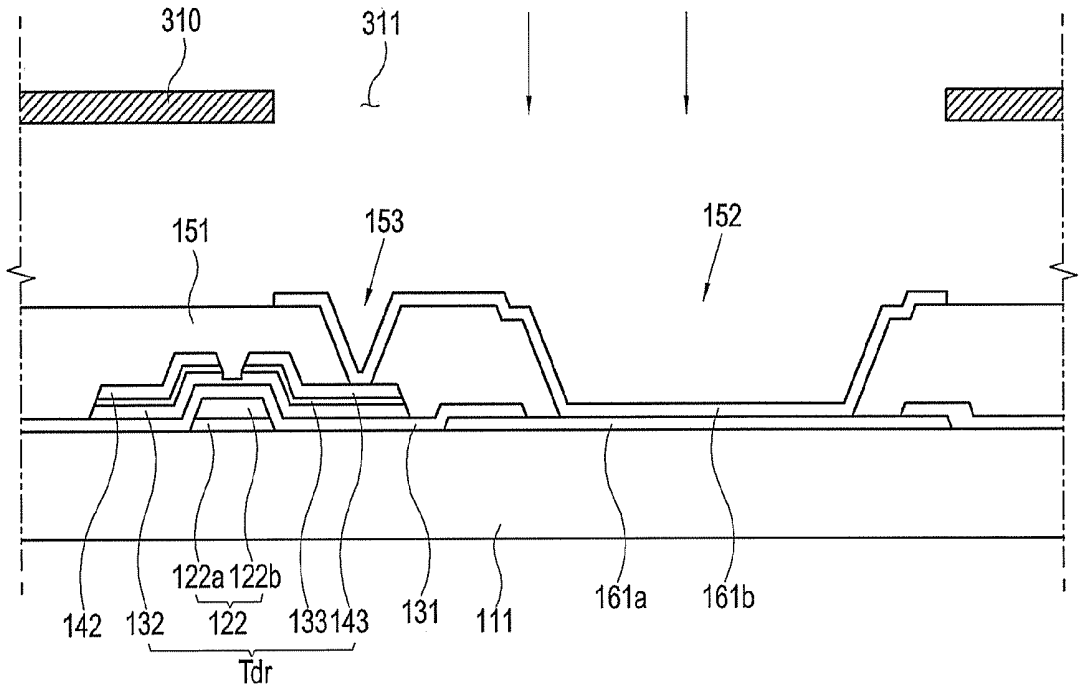

310
311
151
153
152
122a
122b
142
132
122
133
143
131
111
161a
161b
Tdr

FIG. 3M

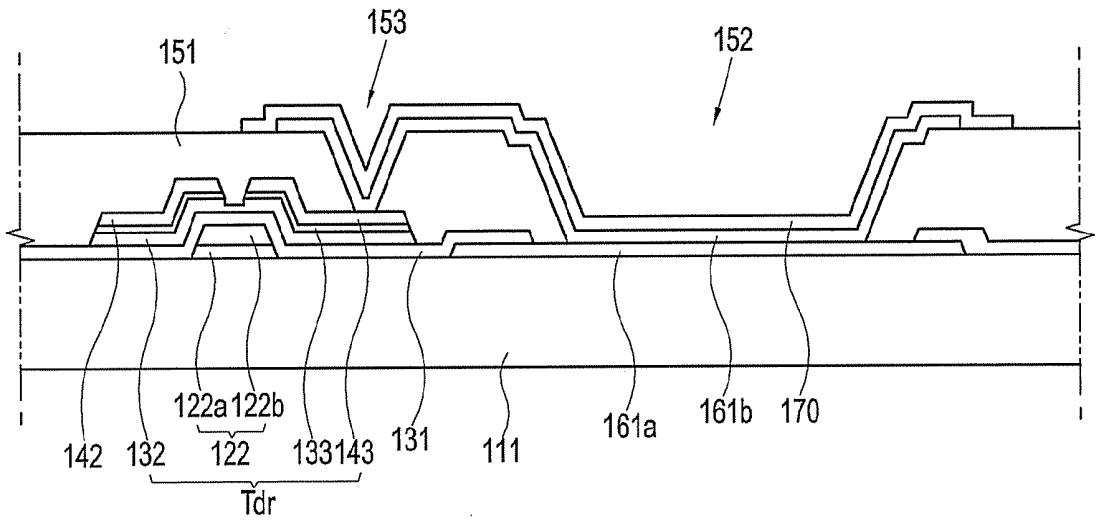

153
151
152
122a
122b
142
132
122
133
143
131
111
161a
161b
170
Tdr

FIG. 3N

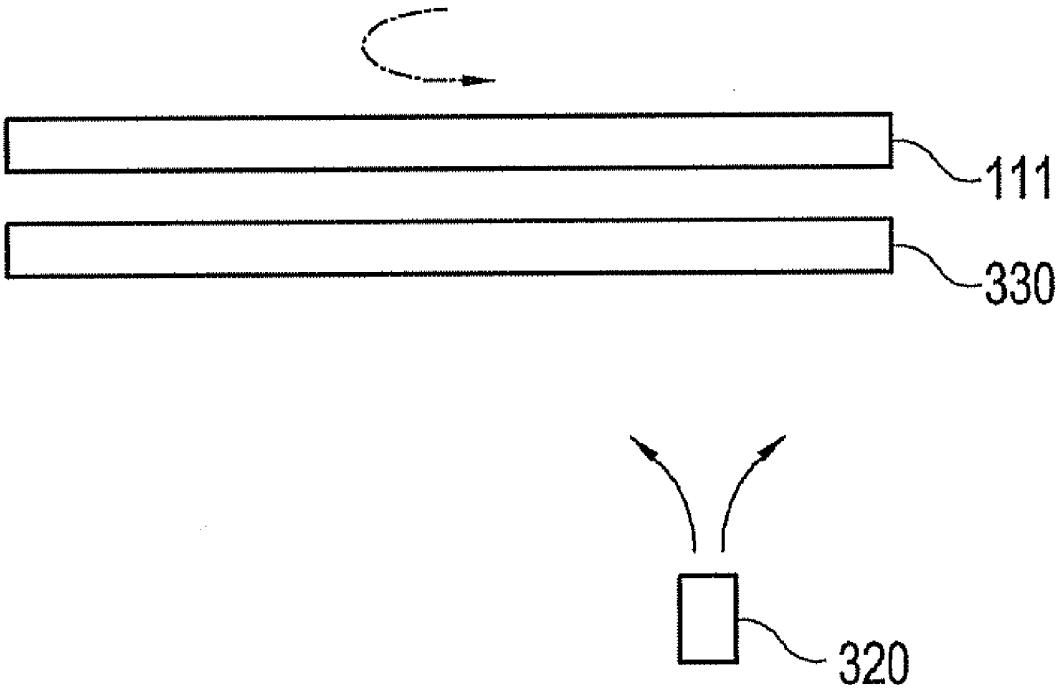


FIG. 4

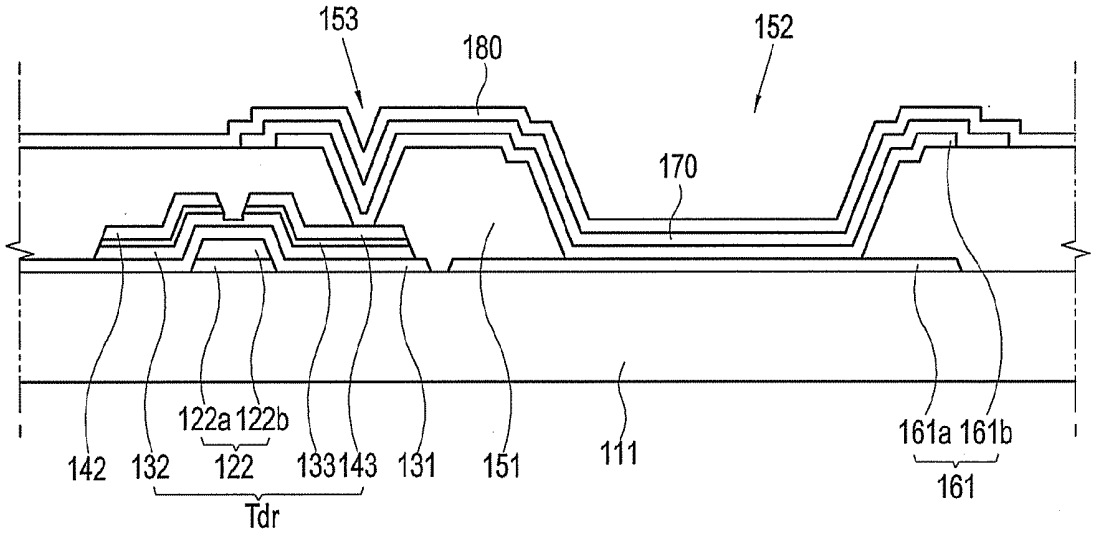

153
180
152
170
122a 122b
142
132
122
133 143
131
151
111
161a 161b
161
Tdr

FIG. 5

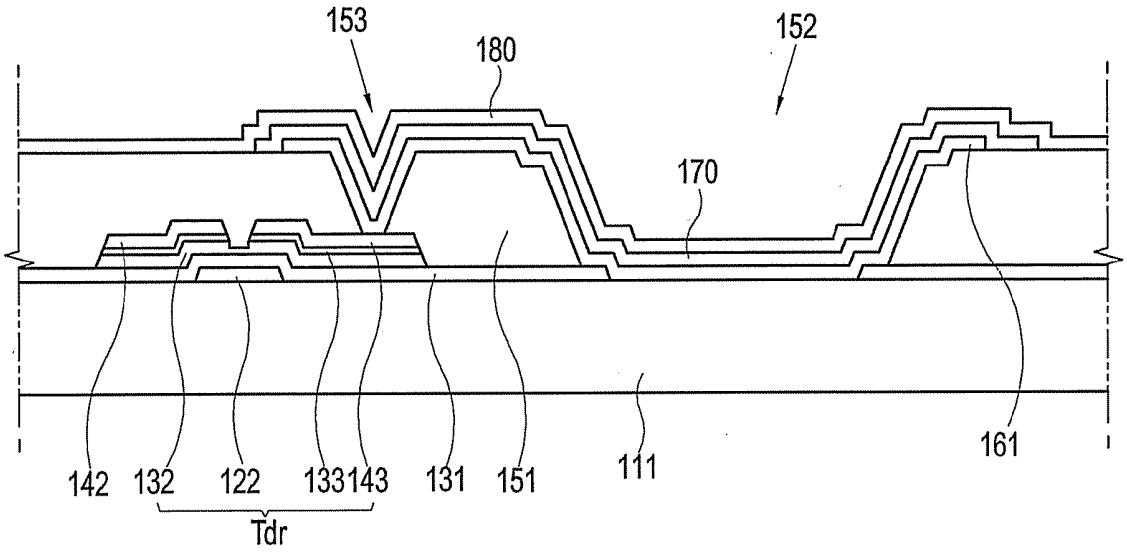


FIG. 6

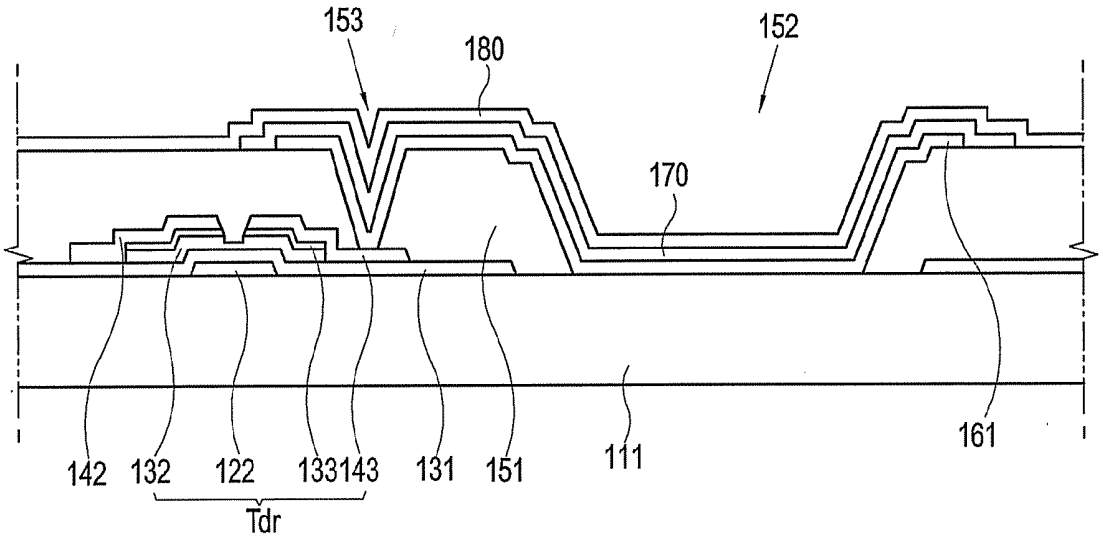
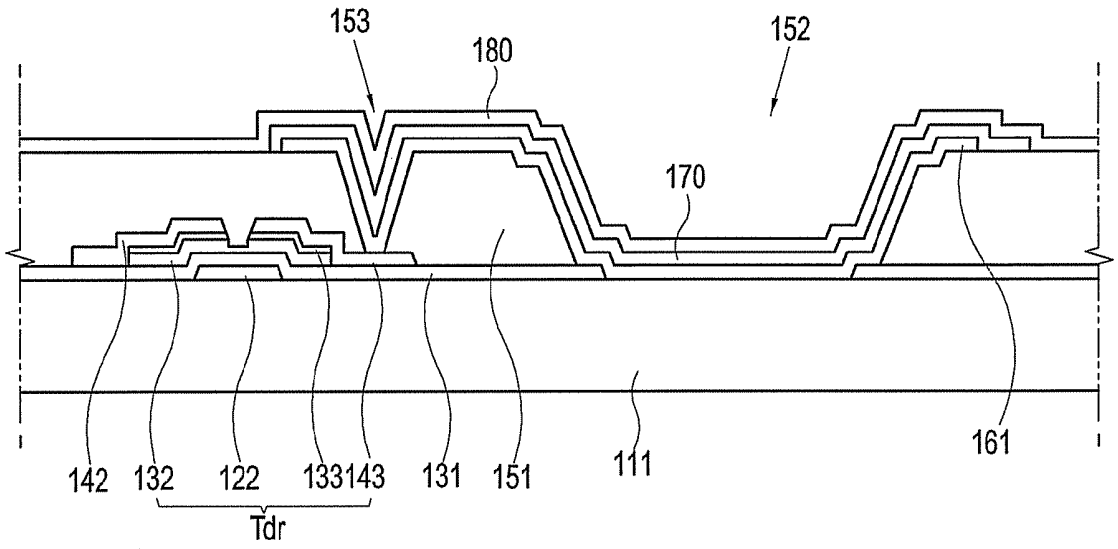


FIG. 7



DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

[0001] This application claims priority to Korean Patent Application No. 2006-0134186, filed on Dec. 26, 2006, and all the benefits accruing therefrom under 35 U.S.C. §119, the contents of which in its entirety are herein incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] (a) Field of the Invention

[0003] The present invention relates to a display device and a method of manufacturing the same, and more particularly, to a bottom emission type display device which emits light from an organic layer to an insulating substrate, and a method of manufacturing the same.

[0004] (b) Description of the Related Art

[0005] Organic light emitting diode ("OLED") displays have recently attracted attention among the wide variety of flat panel displays because they are driven with a low voltage; are thin and lightweight; have a wide view angle; have a relatively short response time; and various other advantageous features.

[0006] OLED displays may be categorized as bottom emission type or top emission type displays according to the direction in which the displays emit light generated from an emission layer to the outside.

[0007] In the case of the bottom emission type OLED display, the light generated from the emission layer is emitted to the outside via an insulating substrate. In such a display an insulating layer and/or an organic layer are interposed between the emission layer and the insulating substrate.

[0008] However, not all of the light generated from the emission layer is passed to the outside; some light is absorbed by the insulating layer and the organic layer. This lowers the light emitting efficiency of the display. Furthermore, color coordinates of the light generated from the emission layer are distorted while passing through the insulating layer and the organic layer.

BRIEF SUMMARY OF THE INVENTION

[0009] Accordingly, it is an aspect of the present invention to provide an exemplary embodiment of a display device having improved light emitting efficiency.

[0010] Another aspect of the present invention is to provide an exemplary embodiment of a method of manufacturing an exemplary embodiment of a display device having improved light emitting efficiency.

[0011] Additional aspects, features and/or advantages of the present invention will be set forth in part in the description which follows and, in part, will be obvious from the description, or may be learned by practice of the present invention.

[0012] An exemplary embodiment of a display device includes; an insulating substrate, a thin film transistor disposed on the insulating substrate and which comprises a drain electrode, a wall disposed on the thin film transistor which includes an opening and a contact hole which exposes the drain electrode, a pixel electrode connected to the drain electrode through the contact hole which comprises a first part in direct contact with the insulating substrate and a second part connected to the first part, an organic layer disposed on the pixel electrode and which comprises an organic emission layer, and a common electrode disposed on the organic layer.

[0013] According to an exemplary embodiment of the present invention, the thin film transistor further comprises an ohmic contact layer disposed below the drain electrode, and the drain electrode and the ohmic contact layer have substantially the same surface area and are disposed above substantially the same region of the insulating substrate.

[0014] According to an exemplary embodiment of the present invention, an edge of the opening is disposed above the first part of the pixel electrode.

[0015] According to an exemplary embodiment of the present invention, an edge of the opening is in direct contact with the insulating substrate.

[0016] According to an exemplary embodiment of the present invention, the display device further comprises an insulating layer disposed between the insulating substrate and the wall, wherein the wall and the insulating layer are in direct contact with each other.

[0017] According to an exemplary embodiment of the present invention, the thin film transistor further comprises a gate electrode, and the insulating layer is disposed between the gate electrode and the drain electrode.

[0018] According to an exemplary embodiment of the present invention, at least a portion of the first part of the pixel electrode is disposed between the insulating substrate and the insulating layer.

[0019] According to an exemplary embodiment of the present invention, at least a portion of the first part of the pixel electrode is disposed between the insulating substrate and the wall.

[0020] According to an exemplary embodiment of the present invention, the gate electrode comprises a lower transparent layer and an upper metal layer.

[0021] According to an exemplary embodiment of the present invention, the pixel electrode disposed between the insulating substrate and the wall has a lower resistance than the pixel electrode connected to the drain electrode.

[0022] According to an exemplary embodiment of the present invention, the common electrode comprises a reflective metal layer.

[0023] An exemplary embodiment of a method of manufacturing a display device, includes; disposing a thin film transistor including a drain electrode on an insulating substrate, disposing a wall on the thin film transistor, the wall comprising an opening and a contact hole which exposes the drain electrode, connecting a pixel electrode to the drain electrode through the contact hole wherein the pixel electrode comprises a first part in direct contact with the insulating substrate and a second part connected to the first part, disposing an organic layer on the first electrode, the organic layer comprising an organic emission layer, and disposing a second electrode on the organic layer.

[0024] According to an exemplary embodiment of the present invention, the disposing the thin film transistor on an insulating substrate includes; disposing a gate electrode on the insulating substrate, disposing an insulating layer on the gate electrode and substantially the entire insulating substrate except a region corresponding to at least a portion of the first part of the pixel electrode, and disposing a semiconductor layer, an ohmic contact layer, a source electrode and the drain electrode on the insulating layer corresponding to the gate electrode.

[0025] According to an exemplary embodiment of the present invention, the wall is disposed directly contacting the source electrode and the drain electrode.

[0026] According to an exemplary embodiment of the present invention, disposing the semiconductor layer, the ohmic contact layer, the source electrode and the drain electrode on the insulating layer includes using a single photolithographic mask.

[0027] According to an exemplary embodiment of the present invention, the connecting of the pixel electrode to the drain electrode is performed using a shadow mask having an opening corresponding to the pixel electrode.

[0028] Another exemplary embodiment of a method of manufacturing an exemplary embodiment of a display device includes; disposing a transparent conductive layer and a metal layer on an insulating substrate, patterning the transparent conductive layer and the metal layer to form a first pixel electrode which comprises the transparent conductive layer and is in direct contact with the insulating substrate, and a gate electrode including the metal layer and the transparent conductive layer, disposing an insulating layer on the insulating substrate, the gate electrode, and at least a portion of the first pixel electrode, disposing a semiconductor layer, an ohmic contact layer, a source electrode and a drain electrode on the insulating layer corresponding to the gate electrode, disposing a wall on a thin film transistor which includes the semiconductor layer, ohmic contact layer, source electrode and drain electrode, the wall including an opening which at least partially exposes the first pixel electrode and a contact hole which exposes the drain electrode, connecting a second pixel electrode to the drain electrode via the contact hole, connecting the second pixel electrode to the first pixel electrode, disposing an organic layer including an organic emission layer on the second pixel electrode, and disposing a common electrode on the organic layer.

[0029] According to an exemplary embodiment of the present invention, the disposing of the wall on the thin film transistor includes disposing the wall in direct contact with the source electrode and the drain electrode.

[0030] According to an exemplary embodiment of the present invention, disposing the semiconductor layer, the ohmic contact layer, the source electrode and the drain electrode on the insulating layer includes using a single photolithographic mask.

[0031] According to an exemplary embodiment of the present invention, the forming of the first pixel electrode includes using a shadow mask having an opening corresponding to the first electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

[0032] The above and/or other aspects and advantages of the present invention will become apparent and more readily appreciated from the following description of the exemplary embodiments, taken in conjunction with the accompanying drawings of which:

[0033] FIG. **1** is an equivalent circuit diagram of a first exemplary embodiment of a display device according to the present invention;

[0034] FIG. **2** is a cross-sectional view of the first exemplary embodiment of a display device according to the present invention;

[0035] FIGS. **3**A through **3**N illustrate an exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device according to the present invention;

[0036] FIG. **4** is a cross-sectional view of a second exemplary embodiment of a display device according to the present invention;

[0037] FIG. **5** is a cross-sectional view of a third exemplary embodiment of a display device according to the present invention;

[0038] FIG. **6** is a cross-sectional view of a fourth exemplary embodiment of a display device according to the present invention; and

[0039] FIG. **7** is a cross-sectional view of a fifth exemplary embodiment of a display device according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0040] The invention now will be described more fully hereinafter with reference to the accompanying drawings, in which embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. Like reference numerals refer to like elements throughout.

[0041] It will be understood that when an element is referred to as being "on" another element, it can be directly on the other element or intervening elements may be present therebetween. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present. As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items.

[0042] It will be understood that, although the terms first, second, third etc. may be used herein to describe various elements, components, regions, layers and/or sections, these elements, components, regions, layers and/or sections should not be limited by these terms. These terms are only used to distinguish one element, component, region, layer or section from another element, component, region, layer or section. Thus, a first element, component, region, layer or section discussed below could be termed a second element, component, region, layer or section without departing from the teachings of the present invention.

[0043] The terminology used herein is for the purpose of describing particular embodiments only and is not intended to be limiting of the invention. As used herein, the singular forms "a", "an" and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. It will be further understood that the terms "comprises" and/or "comprising," or "includes" and/or "including" when used in this specification, specify the presence of stated features, regions, integers, steps, operations, elements, and/or components, but do not preclude the presence or addition of one or more other features, regions, integers, steps, operations, elements, components, and/or groups thereof.

[0044] Furthermore, relative terms, such as "lower" or "bottom" and "upper" or "top," may be used herein to describe one element's relationship to another elements as illustrated in the Figures. It will be understood that relative terms are intended to encompass different orientations of the device in addition to the orientation depicted in the Figures.

For example, if the device in one of the figures is turned over, elements described as being on the "lower" side of other elements would then be oriented on "upper" sides of the other elements. The exemplary term "lower", can therefore, encompasses both an orientation of "lower" and "upper," depending of the particular orientation of the figure. Similarly, if the device in one of the figures is turned over, elements described as "below" or "beneath" other elements would then be oriented "above" the other elements. The exemplary terms "below" or "beneath" can, therefore, encompass both an orientation of above and below.

[0045] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art to which this invention belongs. It will be further understood that terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and the present disclosure, and will not be interpreted in an idealized or overly formal sense unless expressly so defined herein.

[0046] Exemplary embodiments of the present invention are described herein with reference to cross section illustrations that are schematic illustrations of idealized embodiments of the present invention. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected. Thus, embodiments of the present invention should not be construed as limited to the particular shapes of regions illustrated herein but are to include deviations in shapes that result, for example, from manufacturing. For example, a region illustrated or described as flat may, typically, have rough and/or nonlinear features. Moreover, sharp angles that are illustrated may be rounded. Thus, the regions illustrated in the figures are schematic in nature and their shapes are not intended to illustrate the precise shape of a region and are not intended to limit the scope of the present invention.

[0047] Hereinafter, the present invention will be described in detail with reference to the accompanying drawings.

[0048] FIG. **1** is an equivalent circuit diagram of a first exemplary embodiment of a display device according to the present invention.

[0049] The first exemplary embodiment of a display device includes a plurality of pixels. One pixel of the first exemplary embodiment of a display device is provided with a plurality of signal lines. The signal lines include a gate line **121** to transmit a scan signal, a data line **141** to transmit a data signal, and a driving voltage line **144** to transmit a driving voltage. In the present exemplary embodiment, the data line **141** and the driving voltage line **144** are substantially adjacent to and parallel with each other and the gate line **121** extends substantially perpendicularly to the data line **141** and the driving voltage line **144**.

[0050] Each pixel includes an organic light emitting device LD, a switching thin film transistor Tsw, a driving thin film transistor Tdr, and a capacitor C.

[0051] The switching thin film transistor Tsw has a control terminal (gate electrode) connected to the gate line **121**, an input terminal (source electrode) connected to the data line **141**, and an output terminal (drain electrode) connected to the control terminal of the driving thin film transistor Tdr. The switching thin film transistor Tsw transmits the data signal from the data line **141** to the driving thin film transistor Tdr in response to the scan signal applied to the gate line **121**.

[0052] The driving thin film transistor Tdr has a control terminal (gate electrode) connected to the switching thin film transistor Tsw, an input terminal (source electrode) connected to the driving voltage line, and an output terminal (drain electrode) connected to the organic light emitting device LD.

[0053] The capacitor C is connected between the control terminal and the input terminal of the driving thin film transistor Tdr. The capacitor C stores and maintains the data signal to be input to the control terminal of the driving thin film transistor Tdr.

[0054] The organic light emitting device LD has an anode connected to the output terminal of the driving thin film transistor Tdr, and a cathode to which a common voltage is applied. The organic light emitting device LD emits light with a brightness varying according to the intensity of a current output from the driving thin film transistor Tdr. The first exemplary embodiment of a display device may thereby combine the lights emitted from the plurality of pixels to display an image. The intensity of the current output from the driving thin film transistor Tdr varies according to voltages applied between the control terminal and the output terminal of the driving thin film transistor Tdr.

[0055] Below, the first exemplary embodiment of a display device according to the present invention will be described in more detail with reference to FIG. **2**.

[0056] In FIG. **2**, the switching transistor Tsw is not shown, however, exemplary embodiments include configurations wherein it may have a similar structure to the driving transistor Tdr.

[0057] The driving transistor Tdr includes a gate electrode **122** and a first pixel electrode **161***a* is formed on an insulating substrate **111**. The first pixel electrode **161**a and a second pixel electrode **161***b* form a pixel electrode **161**.

[0058] The gate electrode **122** includes a lower layer **122***a* and an upper layer **122***b*. The lower layer **122***a* includes a transparent conductive material, exemplary embodiments of which include indium tin oxide ("ITO"), indium zinc oxide ("IZO"), and other similar materials, and the upper layer **122***b* includes a metal.

[0059] In the present exemplary embodiment the first pixel electrode **161***a* is in direct contact with the insulating substrate **111**, and includes substantially the same material as the lower layer **122***a* of the gate electrode **122**.

[0060] An insulating layer **131** is formed on the gate electrode **122**. The insulating layer **131** includes an inorganic material, exemplary embodiments of which include silicon nitride and other similar materials. The insulating layer **131** exposes and partially overlaps the first pixel electrode **161***a*.

[0061] A semiconductor layer **132** is formed on the insulating layer **131** above the gate electrode **122**, and an ohmic contact layer **133** is formed on the semiconductor layer **132**.

[0062] The ohmic contact layer **133** is divided into two parts with respect to the gate electrode **122**. In one exemplary embodiment the ohmic contact layer **133** is made of n+ silicon or other similar materials.

[0063] In one exemplary embodiment the semiconductor layer **132** and the ohmic contact layer **133** may be made of amorphous silicon, microcrystalline silicon, crystalline silicon (poly silicon) or other similar materials.

[0064] A source electrode **142** and a drain electrode **143** are formed on the ohmic contact layer **133**. The source electrode **142** and the drain electrode **132** are separated from each other across a channel region disposed therebetween.

[0065] In the first exemplary embodiment, the source electrode **142** and the drain electrode **143** overlap the ohmic contact layer **133**. The source electrode **142** and the drain electrode **142** substantially overlap the semiconductor layer **132** except across the channel region.

[0066] A wall **151** is formed on the driving thin film transistor Tdr. In the present exemplary embodiment the wall **151** is in direct contact with the source electrode **142**, the drain electrode **143**, and the insulating layer **131**. In the present exemplary embodiment an additional planarization layer is not used as the pixel electrode **161** is formed on the already planarized insulating substrate **111**.

[0067] The wall **151** is formed with an opening **152** to expose the first pixel electrode **161***a*, and a contact hole **153** to expose the drain electrode **143**. An edge of the opening **152** is in direct contact with the first pixel electrode **161***a*.

[0068] The second pixel electrode **161***b* is formed on the wall **151** and the first pixel electrode **161***a*. The second pixel electrode **161***b* is connected with the drain electrode **143** via the contact hole **153** and extends substantially above the first pixel electrode **161***a*.

[0069] In one exemplary embodiment the second pixel electrode **161***b* may include indium tin oxide ("ITO") or indium zinc oxide ("IZO") or other similar materials. In the present exemplary embodiment the first pixel electrode **161***a* is formed to have a lower electrical resistance than the second pixel electrode **161***b* for reasons described below.

[0070] The pixel electrode **161** has a two-layered structure with the first pixel electrode **161***a* disposed on the bottom and the second pixel electrode **161***b* disposed on top. The pixel electrode **161** is further divided into a first part, which directly contacts the insulating substrate **111**, and a second part, which does not directly contact the insulating substrate **111**.

[0071] The first part corresponds to the "A" and "B" regions of the pixel electrode **161** as shown in FIG. **2**. The region "B" is disposed on at least two sides of the region "A". The first pixel electrode **161***a* is disposed substantially within the first part. Also, the second pixel electrode **161***b* formed in the opening **152** is disposed substantially within the first part. The pixel electrode **161** in the "A" region is left uncovered by the wall **151** by the opening **152**, and the first pixel electrode **161***a* is covered by the wall **151** or the insulating layer **131** or both in the region "B".

[0072] The second part corresponds to a "C" region of the pixel electrode **161** as shown in FIG. **2**. The region "C" is disposed on at least two sides of the region "A". The second pixel electrode **161***b*, which is disposed on the wall **151** and does not directly contact the insulating substrate **111**, is disposed substantially within the second part.

[0073] An organic layer **170** is formed on the pixel electrode **161** and the wall **151**. In the present exemplary embodiment the organic layer **170** includes an organic emission layer. In alternative exemplary embodiments the organic layer may further include an electron injection layer, an electron transport layer, a hole injection layer, a hole transport layer, or various combinations thereof.

[0074] When included, the hole injection layer and the hole transport layer include strong fluorescent amine derivatives. Exemplary embodiments of the fluorescent amine derivatives include triphenyldiamine derivatives, styryl amine derivatives, amine derivatives having an aromatic condensed ring, and various other similar materials.

[0075] When included, one exemplary embodiment of the electron transport layer includes quinoline derivatives. Exemplary embodiments of the electron transport layer may include aluminum tris(8-hydroxyquinoline)(Alq3) as a quinoline derivative. Alternative exemplary embodiments include configurations wherein the electron transport layer includes phenyl anthracene derivatives or tetraarylethen derivatives.

[0076] In one exemplary embodiment the electron injection layer may include barium (Ba) or calcium (Ca).

[0077] In one exemplary embodiment the organic emission layer emits light corresponding to one of a red color, a green color, a blue color and white color. In one such exemplary embodiment neighboring organic emission layers emit light of different colors from each other.

[0078] In an alternative exemplary embodiment the organic emission layer may emit light of the white color. In such an alternative exemplary embodiment a color filter may be provided between the organic layer **170** and an outside.

[0079] The organic layer **170** substantially covers the pixel electrode **161** and prevents short-circuits between the pixel electrode **161** and a common electrode **180**.

[0080] The common electrode **180** is formed on the organic layer **170** and the wall **151**. In one exemplary embodiment the common electrode **180** includes a reflective metal layer.

[0081] A description of the emission of light from the organic layer **170** follows.

[0082] Holes are introduced from the pixel electrode **161** and electrons are introduced from the common electrode **180**. The holes and electrons recombine to form excitons within the organic layer **170**, and photons, which may be perceived by an observer as visible light, are emitted when the excitons de-excite. Alternative exemplary embodiments include configurations wherein holes are introduced from the common electrode **180** and electrons are introduced from the pixel electrode **161**.

[0083] In the current exemplary embodiment the light emitted from the organic layer **170** toward the common electrode **180** is reflected toward the pixel electrode **161**. The pixel electrode **161** is substantially transparent, so that the light from the organic layer **170** is transmitted to the outside through the pixel electrode **161** and the insulating substrate **111**. This is commonly referred to as a bottom-type display.

[0084] In the current exemplary embodiment the light which is emitted to the outside is generated primarily from the "A" region, and that light is not transported through the insulating layer **131**. Therefore, there is no loss of light due to photons passing through the insulating layer **131**, thereby light emitting efficiency is improved. Also, color coordinates of the emitted light are not distorted by passing through the insulating layer **131**.

[0085] Below, an exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device according to the present invention will be described with reference to FIGS. **3**A through **3**N. In the present exemplary embodiment the semiconductor layer **132** and the ohmic contact layer **133** are made of crystalline silicon, and the organic layer **170** is formed by a dry method such as thermal evaporation. Alternative exemplary embodiments include configurations wherein the organic layer **170** may be formed through a wet method such as ink jet printing.

[0086] First, referring to FIG. **3**A, a transparent conductive layer **191** and a metal layer **192** are formed on the insulating substrate **111**. In the present exemplary embodiment the transparent conductive layer **191** and the metal layer **192** are formed by a sputtering method; however, alternative exem-

plary embodiments include configurations wherein the transparent conductive layer **191** and the metal layer **192** are formed by other methods such as chemical vapor deposition ("CVD") and other similar methods. Because the transparent conductive layer **191** is formed on the insulating substrate **111** and the metal layer **192** are formed first, before other more temperature sensitive elements, the transparent conductive layer **191** can be formed at a high temperature resulting in a good quality (e.g., low resistance). The transparent conductive layer **191** may be formed with a very low resistance because at this stage in the manufacturing process no other layers will be harmed by the high temperatures required to generate a low resistance conductive layer. This transparent conductive layer **191** will eventually form the first pixel electrode **161***a*. As will be described in more detail below, the second pixel electrode **161***b* will be formed after more temperature sensitive components have already been formed, and therefore it will not be able to be heated to the same degree, and therefore attain the same low level of resistivity, as the first pixel electrode **161***a*.

[0087] Then, a photoresist layer pattern **211**, **212** is formed as shown in FIG. **3**B. A first photoresist layer pattern **211** corresponds to a position where the gate electrode **122** is to be formed, and a second photoresist layer pattern **212** corresponds to a position where the first pixel electrode **161***a* is to be formed. The first photoresist layer pattern **211** is formed to be thicker than the second photoresist layer pattern **212** for reasons described in more detail below.

[0088] The photoresist layer pattern **211**, **212** is formed by forming a photoresist layer on the metal layer **192** and then exposing and developing the photoresist layer. Exemplary embodiments of the process for forming the photoresist layer include slit coating, spin coating, screen printing, and other similar processes.

[0089] There are various methods of making the photoresist layer pattern **211**, **212** have varying thicknesses according to position. Exemplary embodiments of the various methods include using a mask having a slit, a lattice pattern or a translucent layer to adjust transmissivity with respect to a developing light above the photoresist layer so that a region of the photoresist layer corresponding to the second photoresist layer pattern **212** receives more exposure to the light than the region corresponding to the first photoresist layer pattern **211**, but less exposure than the rest of the photoresist layer which is substantially removed by the developing process. The areas which are fully exposed to the developing light are then removed through a developing process, the areas which are only partially exposed to the developing light are partially removed by the developing process, and the areas which are not exposed to the developing light are not removed by the developing process.

[0090] In the exemplary embodiment wherein a mask with a slit or lattice pattern is used to form the first and second photoresist layer patterns **211** and **212**, a line width of the pattern between the slits or a gap between the patterns, e.g., the width of the slit, is smaller than the resolving power of the exposure system. In other words, the line width of the pattern between the slits or a gap between the patterns allows only a portion of the developing light used in the developing process therethrough resulting in a partial exposure and development. In the exemplary embodiment wherein a mask with a translucent layer is used to form the first and second photoresist layer patterns **211** and **212**, a thin film having different transmissivity or different thickness is used to adjust the transmissivity above the various regions.

[0091] When the photoresist layer is exposed to the light through the mask, a polymer which is directly exposed to the light is completely decomposed, but a polymer corresponding to a slit pattern or a translucent layer is only partially decomposed. Furthermore, the polymer which is substantially covered with a shield layer is not decomposed. When the photoresist layer is developed, only the part where polymers are not decomposed remains, and the thickness of a photoresist layer which was partially exposed to light is less than that of a part which was exposed to no light. When using an exemplary embodiment of a developing mask as described above all polymers may become decomposed if the exposure time exceeds a certain amount. Therefore, the exposure time should be adjusted to take this into consideration.

[0092] Next, as shown in FIG. **3**C, the metal layer **192** and the transparent conductive layer **191**, which are not covered with the photoresist layer pattern **211** and **212**, are etched and removed using the first and second photoresist layer patterns **211**, **212** as a mask. In this stage, the thickness of the photoresist pattern **211** and **212** is decreased due to the etching process.

[0093] Thus, the gate electrode **122** and the first pixel electrode **161***a* are formed. Here, a patterned metal layer **192***a* remains on the first pixel electrode **161***a*.

[0094] Then, as shown in FIG. **3**D, the photoresist layer patterns **211** and **212** undergo ashing, and the second photoresist pattern **212** is removed to thereby expose the patterned metal layer **192***a*. In this stage, the thickness of the first photoresist layer pattern **211** is decreased by the ashing by at leas the thickness of the second photoresist layer **212**. The ashing is performed carefully in order to not remove the first photoresist layer pattern **211**.

[0095] FIG. **3**E illustrates that the exposed patterned-metal layer **192***a* and the remaining first photoresist layer pattern **211** are removed. The removal may be done by any of several well known methods including ashing.

[0096] Then, as shown in FIG. **3**F, the insulating layer **131** is formed on the gate electrode **122** and at least partially on the first pixel electrode **161***a*. Here, an insulating material layer, exemplary embodiments of which include silicon nitride, is formed on substantially the entire surface of the insulating substrate **111**, and then the insulating material layer is photolithographed, thereby forming the insulating layer **131** as seen in FIG. **3**F. In one exemplary embodiment the insulating material can be formed by CVD.

[0097] The insulating layer **131** surrounds the first pixel electrode **161***a* but leaves a relatively large part of the first pixel electrode **161***a* uncovered.

[0098] Then, as shown in FIG. **3**G, a semiconductor material layer **193**, an ohmic contact material layer **194**, a metal layer **195** are formed in sequence. Then, a third photoresist layer pattern **213** and a fourth photoresist layer pattern **214** are formed on the metal layer **195**.

[0099] In the present exemplary embodiment the semiconductor material layer **193** and the ohmic contact material layer **194** are made of crystalline silicon.

[0100] In the present exemplary embodiment the semiconductor material layer **193** and the ohmic contact material layer **194** may be formed by crystallizing an amorphous silicon layer (not shown). Exemplary embodiments of the crystallizing method include a solid phase crystallization ("SPC")

method, a laser crystallization method, a rapid thermal annealing ("RTA") method, and various other similar methods.

[0101] Solid phase crystallization ("SPC") is a method of annealing the amorphous silicon for a long time at a low temperature, e.g., lower than 600° F., thereby obtaining crystalline silicon with a large grain size. Laser crystallization includes methods such as excimer laser annealing ("ELA"), sequential lateral solidification ("SLS"), and various other similar techniques, which use a laser for obtaining the crystalline silicon. Rapid thermal annealing ("RTA") is a method which deposits amorphous silicon at a low temperature and than anneals the surface of the amorphous silicon rapidly with light.

[0102] The third photoresist layer pattern **213***is* placed on an area which will become the channel part C of a thin film transistor, e.g., between the source electrode **142** and the drain electrode **143**. The fourth photoresist layer pattern **214** is placed on an area corresponding to the source electrode **142** and the drain electrode **143** of the yet to be formed thin film transistor. In the present exemplary embodiment the third photoresist pattern **213** is thinner than the fourth photoresist pattern **214**.

[0103] A thickness ratio between the photoresist layer patterns **213** and **214** is varied according to conditions in an etching process (to be described later). In one exemplary embodiment the thickness of the third photoresist layer pattern **213** is less than half a thickness of the fourth photoresist layer pattern **214**. For example, the third photoresist layer pattern has a thickness of 4,000 Å or less.

[0104] The different photoresist layer patterns **213** and **214** can be formed by substantially the same method as that shown in FIG. **3**B, and repetitive descriptions thereof will be omitted.

[0105] Then, the semiconductor material layer **193**, the ohmic contact material layer **194** and the metal layer **195** are etched using the photoresist layer patterns **213** and **214** as a mask. Referring to FIG. **3**H, the metal layer **195** not covered by the photoresist layer patterns **213** and **214** is removed, thereby exposing the ohmic contact material layer **194**. At this point in the exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device dry etching and wet etching may be used.

[0106] In one exemplary embodiment the etching is performed under the condition that the metal layer **195** is etched but the photoresist layer pattern **213**, **214** are not decreased in thickness by the etching. However, in the exemplary embodiment wherein dry etching is used it is difficult to control the etching process so that only the metal layer **195** is etched without etching the photoresist layer patterns **213**, **214**. Therefore in the exemplary embodiment using dry etching the photoresist layer pattern **213**, **214** are etched together with the metal layer **195**.

[0107] Accordingly, in the exemplary embodiment using dry etching, the third photoresist layer pattern **213** is formed to be substantially thicker than the third photoresist layer pattern **213** in exemplary embodiment using wet etching, thereby preventing the third photoresist layer pattern **213** from being removed and the metal layer **195** below from being exposed.

[0108] In the present exemplary embodiment the patterned metal layer **195***a* is not yet divided into the source electrode **142** and the drain electrode **143**.

[0109] As shown in FIG. **3**I, the exposed ohmic contact material layer **194** and the semiconductor material layer **193** are removed with the third photoresist layer pattern **213** by the dry etching.

[0110] In the present exemplary embodiment the dry etching is performed so that the photoresist layer patterns **213**, **214**, the ohmic contact material layer **194**, and the semiconductor material layer **193** are removed at substantially the same time, while leaving the insulating layer **131** substantially untouched by the etching. In one exemplary embodiment an etching rate of the photoresist layer pattern **213**, **214** is substantially equal to that of the semiconductor material layer **193**.

[0111] Referring to FIG. **3**I, the third part **213** is removed to expose the patterned metal layer **195***a* above the channel area of the yet to be formed thin film transistor, and a patterned ohmic contact material layer **194***a* and a patterned semiconductor material layer **193***a* are provided in substantially the same area as the patterned metal layer **195***a*.

[0112] In this stage in the exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device the patterned ohmic contact material layer **194***a* is not yet divided into two parts. Furthermore, in this stage, the thickness of the fourth photoresist layer pattern **214** is decreased due to the etching. Also in this stage any photoresist layer waste remaining on the metal layer **195***a* exposed in the channel area is removed. In one exemplary embodiment it may be removed by ashing.

[0113] Referring to FIG. **3**J, the patterned metal layer **195***a* in the channel area, and the patterned ohmic contact material layer **194***a* disposed below are etched and removed.

[0114] The etching removes the metal layer **195** and the ohmic contact material layer **194** and leaves the semiconductor material layer **193** on the area which was covered by the third photoresist layer pattern **213**. The etching leaves the semiconductor material layer **193**, the ohmic contact material layer **194** and the metal layer **195** on the area covered by the fourth photoresist layer pattern **214**.

[0115] Because the patterned ohmic contact material layer **194***a* is relatively thin, it may be relatively difficult to stop the etching process so that it finishes precisely when all of the ohmic contact material layer **194***a* is removed. Therefore, it is possible that a portion of the patterned semiconductor layer **193***a* is partially removed as shown in FIG. **3**J. Therefore, the thickness of the semiconductor layer **132** may be decreased, and the thickness of the third photoresist layer pattern **214** is also decreased by a relatively small amount.

[0116] At this stage in the exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device the etching is performed without etching the insulating layer **131**. Furthermore the etching is performed carefully so as not to remove the fourth photoresist layer pattern **214** and etch the underlying layers.

[0117] At this stage in the exemplary embodiment of a method of manufacturing the first exemplary embodiment of a display device the now separated patterned metal layer **195***a* forms the source electrode **142** and the drain electrode **143**, the now separated patterned ohmic contact material layer **194***a* forms the ohmic contact layer **133**, and the semiconductor layer **132** is completed.

[0118] Then, the fourth photoresist layer pattern **214** is removed, thereby completing the driving thin film transistor Tdr. Although not shown, a similar process may be used to form the switching thin film transistor Tsw.

[0119] Next, the wall **151** is formed as shown in FIG. **3**K. In one exemplary embodiment the wall **151** is formed by forming a photoresist layer and then exposing and developing the photoresist layer. The wall **151** is formed with the opening **152** to expose the first pixel electrode **161***a* and the contact hole **153** to expose the drain electrode **143**.

[0120] Referring to FIG. **3**L, the second pixel electrode **161***b* is formed on the wall **151**, drain electrode **143** and first pixel electrode **161***a*. In one exemplary embodiment the second pixel electrode **161***b* is formed by a sputtering or thermal evaporation method after disposing a shadow mask **310** in front of the wall **151**.

[0121] The shadow mask **310** is formed with an opening **311** corresponding to a region where the second pixel electrode **161***b* is to be formed. Thus, the second pixel electrode **161***b* is formed on a region exposed through the opening **311**, and the second pixel electrode **161***b* is not formed on a region which is substantially covered with the shadow mask **310**.

[0122] Then, referring to FIGS. **3**M and **3**N, an organic layer **170** is formed on the wall **151** and the second pixel electrode **161***b*. In the present exemplary embodiment the organic layer **170** includes a plurality of layers including an organic emission layer, which is formed by a thermal evaporation method shown in FIG. **3**N. Alternative exemplary embodiments include configurations wherein the organic layer **170** is formed by other methods such as ink-jet printing.

[0123] In the thermal evaporation method, the insulating substrate **111** is disposed with the pixel electrode **161** facing downward, and an organic source **320** under the insulating substrate **110** is heated to supply organic vapor to the insulating substrate **111**.

[0124] A shadow mask **330** is placed between the insulating substrate **111** and the organic source **320**. The shadow mask **300** is formed with an opening (not shown), which may be larger than the second pixel electrode **161**.

[0125] The organic vapor supplied from the organic source **320** is supplied to the second pixel electrode **161***b* and the wall **151** through the opening of the shadow mask **330**. The organic vapor, which contacts either the second pixel electrode **161***b* or the partition wall **151**, or both, decreases in temperature and is solidified into the organic layer **170**.

[0126] In one exemplary embodiment the insulating substrate **111** rotates while forming the organic layer **170**.

[0127] The organic layer **170** shown in the first exemplary embodiment of a display device is formed using the shadow mask. Alternative exemplary embodiments include configurations wherein an open mask is used and the organic layer **170** is formed on substantially the entire surface of the wall **151**. Furthermore, alternative exemplary embodiments include configurations wherein some layers of the organic layer **170** are formed by the open mask, and other layers are formed by the shadow mask.

[0128] Then, a common electrode **180** is formed to thereby complete a first exemplary embodiment of a display device as shown in FIG. **2**.

[0129] In the foregoing exemplary embodiment of a method of manufacturing a first exemplary embodiment of a display device, the photoresist layer patterns **213** and **214**, which are used in forming the semiconductor layer **132**, the ohmic contact layer **133**, the source electrode **142** and the drain electrode **143**, are provided through the use of a single mask.

[0130] According to the exemplary embodiment of a method of manufacturing a first exemplary embodiment of a display device according to the present invention, a planarization layer and a passivation layer are not employed so that a process of patterning the planarization layer and the passivation layer is not required.

[0131] Furthermore, the second pixel electrode **161***b* is formed through the shadow mask **310**, so that there a separate patterning process for the second pixel electrode **161***b* is not required.

[0132] Accordingly, the present invention simplifies a method of manufacturing the exemplary embodiment of a display device.

[0133] A second exemplary embodiment a display device according to the present invention will be described with reference to FIG. **4**.

[0134] In the second exemplary embodiment, the insulating layer **131** is spaced apart from the first pixel electrode **161***a*. An upper surface of the first pixel electrode **161***a* around the opening **152** is in contact with the wall **151**.

[0135] A third exemplary embodiment of a display device according to the present invention will be described with reference to FIG. **5**.

[0136] In the third exemplary embodiment, the pixel electrode **161** is made of a single layer. Furthermore, the pixel electrode **161** is not disposed under the insulating layer **131** or the wall **151**.

[0137] Accordingly, the method of manufacturing the pixel electrode **161** can be simplified.

[0138] A fourth exemplary embodiment of a display device according to the present invention will be described with reference to FIG. **6**.

[0139] In the fourth exemplary embodiment, the source electrode **142** and the drain electrode **143** extend beyond the ohmic contact layer **133**. In other words, the source electrode **142** and the drain electrode **143** are formed throughout a region larger than the ohmic contact layer **133**.

[0140] In the fourth exemplary embodiment the source electrode **142** and the drain electrode **143** are formed by a separate photolithography step after the photolithographic forming of the ohmic contact layer **133**.

[0141] In the fourth exemplary embodiment the pixel electrode **161** is provided as a single layer, and the edge of the opening **152** of the wall **151** is in direct contact with the insulating substrate **111**.

[0142] A fifth exemplary embodiment of a display device according to the present invention will be described with reference to FIG. **7**.

[0143] In the fifth exemplary embodiment, the source electrode **142** and the drain electrode **143** extend beyond the ohmic contact layer **133** as described with respect to the fourth exemplary embodiment.

[0144] The pixel electrode **161** is provided as a single layer, and the edge of the opening **152** is in direct contact with the insulating layer **131**.

[0145] As described above, the present invention provides a display device having improved light emitting efficiency and a method of manufacturing the same.

[0146] Although a few exemplary embodiments of the present invention have been shown and described, it will be appreciated by those skilled in the art that changes may be made in these exemplary embodiments without departing from the principles and spirit of the invention, the scope of which is defined in the appended claims and their equivalents.

What is claimed is:

1. A display device comprising:
an insulating substrate;
a thin film transistor disposed on the insulating substrate and which comprises a drain electrode;
a wall disposed on the thin film transistor and which includes an opening and a contact hole which exposes the drain electrode;
a pixel electrode connected to the drain electrode through the contact hole, and which comprises a first part in direct contact with the insulating substrate and a second part connected to the first part;
an organic layer disposed on the pixel electrode and which comprises an organic emission layer; and
a common electrode disposed on the organic layer.

2. The display device according to claim 1, wherein the thin film transistor further comprises an ohmic contact layer disposed below the drain electrode, and
the drain electrode and the ohmic contact layer have substantially the same surface area and are disposed above substantially the same region of the insulating substrate.

3. The display device according to claim 1, wherein an edge of the opening is disposed above the first part of the pixel electrode.

4. The display device according to claim 1, wherein an edge of the opening is in direct contact with the insulating substrate.

5. The display device according to claim 1, further comprising an insulating layer disposed between the insulating substrate and the wall,
wherein the wall and the insulating layer are in direct contact with each other.

6. The display device according to claim 5, wherein the thin film transistor further comprises a gate electrode, and
the insulating layer is disposed between the gate electrode and the drain electrode.

7. The display device according to claim 6, wherein at least a portion of the first part of the pixel electrode is disposed between the insulating substrate and the wall.

8. The display device according to claim 7, wherein the pixel electrode disposed between the insulating substrate and the wall has a lower resistance than the pixel electrode connected to the drain electrode.

9. The display device according to claim 6, wherein the gate electrode comprises a lower transparent layer and an upper metal layer.

10. The display device according to claim 5, wherein at least a portion of the first part of the pixel electrode is disposed between the insulating substrate and the insulating layer.

11. The display device according to claim 1, wherein the common electrode comprises a reflective metal layer.

12. A method of manufacturing a display device, comprising:
disposing a thin film transistor including a drain electrode on an insulating substrate;
disposing a wall on the thin film transistor, the wall comprising an opening and a contact hole which exposes the drain electrode;
connecting a pixel electrode to the drain electrode through the contact hole wherein the pixel electrode comprises a first part in direct contact with the insulating substrate and a second part connected to the first part;
disposing an organic layer on the first electrode, the organic layer comprising an organic emission layer; and
disposing a second electrode on the organic layer.

13. The method according to claim 12, wherein the disposing the thin film transistor on an insulating substrate comprises:
disposing a gate electrode on the insulating substrate;
disposing an insulating layer on the gate electrode and substantially the entire insulating substrate except a region corresponding to at least a portion of the first part of the pixel electrode; and
disposing a semiconductor layer, an ohmic contact layer, a source electrode and the drain electrode on the insulating layer corresponding to the gate electrode.

14. The method according to claim 13, wherein the wall is disposed directly contacting the source electrode and the drain electrode.

15. The method according to claim 13, wherein disposing the semiconductor layer, the ohmic contact layer, the source electrode and the drain electrode on the insulating layer includes using a single photolithographic mask.

16. The method according to claim 12, wherein the connecting of the pixel electrode to the drain electrode is performed using a shadow mask having an opening corresponding to the pixel electrode.

17. A method of manufacturing a display device, comprising:
disposing a transparent conductive layer and a metal layer on an insulating substrate;
patterning the transparent conductive layer and the metal layer to form a first pixel electrode which comprises the transparent conductive layer and is in direct contact with the insulating substrate, and a gate electrode including the metal layer and the transparent conductive layer;
disposing an insulating layer on the insulating substrate, the gate electrode, and at least a portion of the first pixel electrode;
disposing a semiconductor layer, an ohmic contact layer, a source electrode and a drain electrode on the insulating layer corresponding to the gate electrode;
disposing a wall on a thin film transistor which includes the semiconductor layer, ohmic contact layer, source electrode and drain electrode, the wall including an opening which at least partially exposes the first pixel electrode and a contact hole which exposes the drain electrode;
connecting a second pixel electrode to the drain electrode via the contact hole;
connecting the second pixel electrode to the first pixel electrode;
disposing an organic layer including an organic emission layer on the second pixel electrode; and
disposing a common electrode on the organic layer.

18. The method according to claim 17, wherein the disposing the wall on the thin film transistor includes disposing the wall in direct contact with the source electrode and the drain electrode.

19. The method according to claim 17, wherein disposing the semiconductor layer, the ohmic contact layer, the source electrode and the drain electrode on the insulating layer includes using a single photolithographic mask.

20. The method according to claim 17, wherein the forming of the first pixel electrode includes using a shadow mask having an opening corresponding to the first electrode.

* * * * *

专利名称(译)	显示装置及其制造方法		
公开(公告)号	US20080150434A1	公开(公告)日	2008-06-26
申请号	US11/843210	申请日	2007-08-22
[标]申请(专利权)人(译)	三星电子株式会社		
申请(专利权)人(译)	SAMSUNG ELECTRONICS CO.，LTD.		
当前申请(专利权)人(译)	三星DISPLAY CO.，LTD.		
[标]发明人	SUNG UN CHEOL CHUNG JIN KOO RHEE JUNG SOO		
发明人	SUNG, UN-CHEOL CHUNG, JIN-KOO RHEE, JUNG-SOO		
IPC分类号	G09G3/10 H01L21/84		
CPC分类号	H01L27/1214 H01L27/3244 H01L27/3246 H01L27/1288 H01L29/4908 H01L51/5203 H01L51/5206 H01L27/3248 H01L51/5215		
优先权	1020060134186 2006-12-26 KR		
其他公开文献	US7884542		
外部链接	Espacenet USPTO		

摘要(译)

一种显示装置，包括：绝缘基板，设置在绝缘基板上的薄膜晶体管，包括漏电极，设置在薄膜晶体管上的壁，包括开口和暴露漏电极的接触孔，连接到漏极的像素电极电极穿过接触孔并且包括与绝缘基板直接接触的第一部分和连接到第一部分的第二部分，设置在像素电极上并且包括有机发光层的有机层和设置在其上的公共电极有机层